INTEGRATED CIRCUIT POWER MANAGEMENT FOR REDUCING LEAKAGE CURRENT IN CIRCUIT ARRAYS AND METHOD THEREOF

Abstract of the Disclosure

Leakage current is eliminated in a memory array during a low power mode of a processing system having a processor that interfaces with the memory array. Because two power planes are created, the processor may continue executing instructions using a system memory while bypassing the memory array when the array is powered down. A switch selectively removes electrical connectivity to a supply voltage terminal in response to either processor-initiated control resulting from execution of an instruction or from a source originating in the system somewhere else than the processor. Upon restoration of power to the memory array, data may or may not need to be marked as unusable depending upon which of the two power planes supporting arrays to the memory array are located. Predetermined criteria may be used to control the timing of the restoration of power. Multiple arrays may be implemented to independently reduce leakage current.